Pradyun Narkadamilli

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EDUCATION

University of Illinois Urbana-Champaign, Bachelor of Science in Computer Engineering   4.0/4.0 GPA, May 2025
Bradley J. Griffis Endowed Scholarship, John and Sheila Woythal Scholarship
IEEE HKN Honor Society, Dean's List (Fall 2021-Present)

Ongoing Coursework: Communication Networks, Parallel Programming, Algorithms
Relevant Coursework: Advanced Computer Architecture, VLSI Design, Digital IC Design, Operating Systems,
Vector Space Signal Processing, Digital Signal Processing, Analog Signal Processing, Data Structures

EXPERIENCE

Silicon Engineering Intern (Fabric IP Design Team), Microsoft   May 2024 – Aug 2024
- Developed scheduler subsystem to mitigate power rail droop during mesh packet transmission on Cobalt SoC
- Designed and implemented RTL modules to aggregate and regulate traffic/system events across fabric mesh
- Implemented more robust error checking and template generation within in-house automation tool
- Migrated various release-time packaging deliverables to reusable targets for in-house automation tool

Hardware Engineering Intern, IMC Trading   Jun 2023 – Aug 2023
- Developed system to filter/publish critical network messages to host from FPGA, reducing PCIe load by 50%
- Designed and implemented RTL modules to unpack, tag, and arbitrate between multiple UDP streams
- Created testbenches on Verilator-based verification stack, then prototyped C++ API for new networking interface

Computer Architecture Course Assistant, UIUC   Feb 2024 – Present
- Developed tooling and supported office hours for the projects in UIUC's capstone computer engineering course
- Mentored and evaluated performance targets for 10+ students in the construction of an out-of-order RISC-V core
- Ported existing simulation models and tooling to Verilator, yielding over 200x speedup in processor benchmarking

Operating Systems Course Assistant, UIUC   Aug 2023 – Present
- Conducted office hours for class projects (ex: IA-32 toy kernel) and led exam review sessions for 150+ students
- Developed tooling and infrastructure when migrating kernel development project from IA-32 to RV64 architecture
- Composed course materials like course notes, exam problems, review materials, etc.

Officer, ACM SIGArch sigarch.net   Dec 2023 – Present
- Curated, created, and presented educational material for UIUC's premier computer architecture club.

Digital Systems and FPGA Course Assistant, UIUC   Jan 2023 – Feb 2024
- Created course documentation/resources for SystemVerilog, verifying designs in simulation, and FPGA testing
- Hosted office hours for course's FPGA projects, notable examples include VGA text controller and toy processor

PROJECTS

Trident
Created a superscalar speculative out-of-order RISC-V CPU, implementing the RV32IM spec.
- Supports 1-8 issues/instruction commits per cycle, multiple integer execution units, variable size issue queues, etc.
- Optional parameters to change issue queue scheduling, branch predictor (TAGE), cache timing/associativity, etc.
- Synthesized dual-issue/commit core with L1 cache on FreePDK's 45nm process node at 800MHz
- Created custom standard library cells and layout for a single-commit variation on FreePDK's 45nm process node

NES Emulator pradyun.tech/work/naes
Replicated commercial Nintendo Entertainment System (NES) SoC on DE-10 Lite FPGA.
- System can play standard iNES-formatted ROMs on a Motorola 6502 core, video output is displayed over VGA
- Designed PPU (architecture-specific GPU), peripheral emulation hardware, and memory interfaces
- Demoed at ECE 385 Showcase, running games like Ice Climber, Pac-Man, and Super Mario Bros.

Linux-Like x86 Kernel
Designed and implemented kernel from scratch for use with single-core x86 systems.
- Functionalities: Paging-only virtual memory, read-only filesystem compatibility, round-robin scheduler
- Capabilities: Up to 10 interactive shells concurrently, keyboard/mouse support, running a POSIX-like shell

TECHNICAL SKILLS

General: SystemVerilog, Verilog, Python, C, C++, [ba]sh scripting, Rust, Linux Systems, x86, RISC-V, CUDA
Tools: Synopsys VCS, Verdi, Design Compiler, Virtuoso, Innovus, Verilator, Vivado, Quartus, gem5, git